NARAYANA ENGINEERING COLLEGE::NELLORE

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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

PAPER PUBLICATIONS

Academic Year: 2014-15

S.No	Name of the Authors	Title of Paper	Name of the Journal	Year of Publication	ISBN/ISSN No.
1.	Subba Reddy Borra, G.Jagadeeswar Reddy, E. Sreenivasa Reddy	Fingerprint Image Compression Using Wave Atom Transform	International Journal of Advanced Computing,	April 2015	2051- 0845
2.	Afroz Shaik, M.Chandra Mohan Reddy, C.Leela Mohan, D.Naveena	Single Phase Clock Distribution for Multiband Frequency Divider	Global Journal For Research Analysis (GJRA)	May 2015	2051- 0845
3.	A. Dayakar, C. Leela Mohan, J. Jagadish, M. Anitha	An Efficient Design of 16-Bit SQRT Carry Select Adder for Low Carry Propagation Delay	Global Journal For Research Analysis (GJRA)	May 2015	2051- 0845
4.	Sindhu.A, Penchalaiah.K	Low-Power DSP Architecture Folded Tree for WSN By Using Prefix operations	Global Journal For Research Analysis (GJRA)	May 2015	2051- 0845
5.	D. Naveena, SK. Sabiha, Y. Pallavi, B.V.S.LakshmiSindhura	Architecture for Matching of Data Encoded With Schematic Error Correcting Codes-A Reduced Delay Version	Global Journal For Research Analysis (GJRA)	May 2015	2051- 0845
6.	J.Jagadish, C.Leela Mohan, K.Sai Sandeep, A.Dayakar	Design of 64-Bit Hybrid Adder by Using Radix-4 Prefix Tree Structure	Global Journal For Research Analysis (GJRA)	May 2015	2051- 0845
7.	K. Spurthi, K. Murali, M. V. Srinivasa Reddy, B. V. S. Lakshmi Sindhura	I2C on an FPGA - A Verification of Communication Protocol	Global Journal For Research Analysis (GJRA)	May 2015	2051- 0845
8.	K. Umamaheswari, S. Girish Gandhi, T. Mounika	An Accommodative Adaptive FIR Filter Design Based on Distributed Arithmetic	Global Journal For Research Analysis (GJRA)	May 2015	2051- 0845
9.	K. Sai Sandeep, C. Leela Mohan, B.V.S. Lakshmi Sindhura, SK. Afroz	Radix-10 Multiplication Using Redundant BCD Codes - A High Speed Version	Global Journal For Research Analysis (GJRA)	May 2015	2051- 0845
10.	Suma Rani.N, Muralidhar.M, Pavani.,Sumanth.V	A Reliable ALU Based Test Pattern Generation for VLSI Chips	Global Journal For Research Analysis (GJRA)	May 2015	2051- 0845

11.	Sk. Firoz, S. Girish Gandhi, C. Leela Mohan, M. Swarna Lakshmi	Sectional Reconfigurable FIR Filter Design Using Systolic Distributed Arithmetic (DA) Architecture On FPGA	Global Journal For Research Analysis (GJRA)	May 2015	2277 - 8160
12.	T.Pavani, M.C.M.Reddy, N.Sumarani, T.Mounika	Design of BIST Enabled UART using Cellular Automata LFSR	Global Journal For Research Analysis (GJRA)	May 2015	2277 - 8160
13.	T.Mounika, Sk.Shaguftha, K.Umamaheswari, T.Pavani	High Performance and High Energy-Efficient pulsed Latches	Global Journal For Research Analysis (GJRA)	May 2015	2277 – 8160
14.	B.V.S. Lakshmi Sindhura, J. Sunil Kumar, M.V. Srinivasa Reddy, K. Spurthi	FPGA based Mechanized Vending Machine With Multi Select and Cancel Attributes	Global Journal For Research Analysis (GJRA)	May 2015	2277 – 8160
15.	Y. Pallavi, J. Sunil Kumar, D. Naveena, SK. Firoz	Design of Add-Multiply operator Using an optimized and Modified Booth Recorder	Global Journal For Research Analysis (GJRA)	May 2015	2277 – 8160
16.	Lavanya.CH, Girish Gandhi .S	Efficient Fixed Point LMS Adaptive Filter Implementation on FPGA	Global Journal For Research Analysis (GJRA)	May 2015	2277 – 8160
17.	Ch.Leela, K.Murali	Shadow Detection and Removal Caused by Manmade Buildings In High Resolution Remote Sensing Images	Global Journal For Research Analysis (GJRA)	May 2015	2277 – 8160
18.	CH. Sandhya Rani, M. Muralidhar	Implementation of High Speed 8-Bit Vedic Multiplier using Barrel Shifter by Employing CPLDs	Global Journal For Research Analysis (GJRA)	May 2015	2277 – 8160
19.	K. Jaya Raju, Syed Athika sultana	Morphological Process for Detection of Exudates In Digital Retinal Images	Global Journal For Research Analysis (GJRA)	May 2015	2277 – 8160
20.	K.Kiran Kumar Reddy, J.Sunil Kumar	Image Enhancement Different Lighting Conditions using Colour and Depth Image	Global Journal For Research Analysis (GJRA)	May 2015	2277 – 8160
21.	M. Jhansi, K. Murali, M. Srinivasulu	Hardware-In-The-Loop (HIL) Simulation for Automative Electronic Control Unit (ECU)	Global Journal For Research Analysis (GJRA)	May 2015	2277 – 8160
22.	N.Sumedha Sherly, P.Sindhuri	A Secret Sharing Method Via Secret-Fragment visible-Mosaic Image	Global Journal For Research Analysis (GJRA)	May 2015	2277 – 8160

23.	P.Shalinivishnupriya, K.S.Sagar Reddy	Performance Improvement in MANET using Neural Network	Global Journal For Research Analysis (GJRA)	May 2015	2277 – 8160
24.	Shaik.Kamila, M.praveen Kumar	Fully Reused VLSI Architecture of FMO/Manchester Encoding Using SOLS Technique for DSRC Applications	Global Journal For Research Analysis (GJRA)	May 2015	2277 - 8160
25.	S.Bindhu, P.Sravan Kumar	Analysis of Throughput Performance of Mobile Ad-Hoc Networks under NS2	Global Journal For Research Analysis (GJRA)	May 2015	2277 - 8160
26.	S.PenchalaPrasad, K.Murali	Automatic Skin Lesion Classification using Hybrid Features Extraction And Artificial Neural Network	Global Journal For Research Analysis (GJRA)	May 2015	2277 - 8160
27.	T Sai Yagnesh Singh, K S Sagar Reddy	Enhancing The QOS Using AODV and DSDV Protocols In MANETs Based on Energy Consumption	Global Journal For Research Analysis (GJRA)	May 2015	2277 - 8160
28.	Y Sai Krishna Reddy, Kante Murali	Power-Constrained Contrast Improvement Algorithm Multi Scale Retinex for OLED Display	Global Journal For Research Analysis (GJRA)	May 2015	2277 - 8160
29.	R.LakshmiSwarupa, P.M.Kondaiah, M.Swarnalakshmi	High Power-Efficiency and Good QOS for MIMO- OFDM in Mobile Communications using SVD	Global Journal For Research Analysis (GJRA)	May 2015	2277 - 8160
30.	P Sindhoori, KS Sagar Reddy	An Automated Computer Aided Diagnosis Tool for Breast Tumor Segmentation and Analysis	Global Journal For Research Analysis (GJRA)	May 2015	2277 - 8160
31.	PALLALA PRANAYKUMAR, D.SREELAKSHMI	A Novel VLSI DHT Algorithm for A Highly Modular And Parallel Architecture	International Journal of Scientific Engineering and technology Research	Dec 2014	2319-8885
32.	CH.Manoj Kumar, K. Murali	Design and Comparison of Effective Area Efficient Architectures for CSLA using CLA	International Journal of VLSI System Design and Communication Systems	Aug 2014	2322 - 0929
33.	P. YASWANTH, KANTE MURALI	Power Reduction of Pulse Triggered Flip Flop using Enhanced Pulse	International Journal of VLSI System Design and Communication Systems	Aug 2014	2322 - 0929

34.	G. Lakshminarayana Yadav, P. Sravan Kumar Reddy	A Novel Architecture for High Speed 1-Bit Full Adder at 45nm Technology	IJVES	Sept 2014	2249 - 6556
35.	O.Harish Sk.shaguftha	A Multiband Flexible Integer-N Divider based on pulse swallow topology	IJVES	Sept 2014	2249 - 6556
36.	C LEELAMOHAN,S.UMAMAHESWARARAO	Reducing Area & Increasing Speed using Vedic Multiplier with Compressors	IJECT	Sept 2014	2230-7109
37.	C LEELA MOHAN,CV.KAVYA LA KSHMI	Co-Operative relaying and Orthogonal FDM based Wireless Communication Systems	IJCEA	Dec 2014	2230-8520
38.	C LEELA MOHAN,R.SIVA SAI	A Novel Architecture for MAC Unit Using Reversible Logic Gates	IJVES	Sept 2014	2249-6556
39.	G.sindhura Bhargavi B. praveen kumar T. kalyan	Fast Background Subtraction Algorithm for Moving Object Detection & Tracking In FPGA	IJSHRE	June 2014	2347- 4890
40.	K.S Sagar Reddy, Dr S.Varadarajan	Network Traffic Prediction In 4G Networks Based on Neural Network for Improving QOS	Journal of Theoretical and Applied Information Technology	April 2014	1992- 8645
41.	G.sindhura Bhargavi T.kalyan	Low Power Dynamic Logic Circuit Design Using Footed Diode Domino Logic	IJER	March 2014	2319- 6890
42.	Kante Murali, Ravibabu Mulaveesala, and D. V. Rama Koti Reddy	Non-Destructive Testing by Means of Frequency Modulated Infrared Imaging	International Journal of Computer and Communication Engineering	Nov2013	2010- 3743
43.	Y.Shekar, B.Vasunayak, J.Sunil Kumar, A.Sanyasi Rao, Fathima Shireen	Cryptographic Algorithms Implementation on RISC Processor	IJIES	Nov 2013	2319-9598
44.	P.Sahithi KS. Sagar Reddy, P.Sindhoori,	Roi Segmentation on Lung Ct Images in Noisy Environment	International Journal of Engineering Research & Technology (IJERT)	Sept 2013	2278- 0181
45.	Kiran Kumar.M, Murali Kante, Narayana Reddy Vanteru	High Speed Low Area Pattern Matching Algorithm for Memory Architecture	International Journal of Engineering Sciences & Research Technology	June 2013	2277- 9655
46.	C LEELA MOHAN,M SRILAKSHMI	Implementation of Distributed Canny Edge Detector on FPGA	IJIRSET	July 2013	2319-8753